"LIGHT SPEED — 100"

256K S-100

Disk Simulator

DIGITAL RESEARCH COMPUTERS

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1.1 LIMITED WARRANTY

Read the enclosed yellow sheet for a statement of our limited warranty as related to this kit.

Also note that when this product is purchased as a blank board, all that is covered by the limited warranty is the PC board itself.

Under no circumstance should you cut any traces on the PC board. To do so will VOID your warranty and we will not service any cut or modified board.

1.2 SOFTWARE DISCLAIMER

Digital Research Computers makes no representations or warranties with respect to the software supplied with the LS-100 board and specifically disclaims any implied warranties of merchantability or fitness for any particular purpose. Futher, Digital Research Computers reserves the right to revise the included software from time to time without any obligation of Digital Research Computers to notify any person or organization of such revisions or changes.

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1.3 LS-100 FEATURES

USES FIVE VOLT ONLY 64K x 1 DYNAMIC RAMS

USES INTEL 8203-1 DYNAMIC RAM CONTROLLER

PROVIDES 256K BYTES PER BOARD OF ON LINE STORAGE

REQUIRES ONLY FOUR I/O PORTS FOR OPERATION (DIP SWITCH SELECTABLE)

EXPANSION OF UP TO EIGHT BOARDS PROVIDING 2 MEGABYTES OF STORAGE

INTERFACES WITH 8080 OR Z80 PROCESSOR BOARDS

PROVISION FOR EXTERNAL POWER OR BATTERY BACKUP

BOARD SELECT AND ACCESS STATUS LED INDICATORS

LOW POWER (600 MA. TYPICAL)

DOUBLE SIDED PC BOARD WITH PLATED THROUGH HOLES

SILK SCREENED COMPONENT LEGEND AND SOLDER MASKED

GOLD PLATED FINGERS

FULLY BUFFERED AND BYPASSED

IEEE 696 S-100 BUS COMPATABILE (as proposed)

OVERLAY,FORMATTER, AND DIAGNOSTIC SOFTWARE PROVIDED (CP/M 2.2 REQ.)

1.4 OVERVIEW

The LS-100 board is a high density memory board that is organized as an array of four banks by eight bits of 64K dynamic rams. The LS-100 provides the user with a total of 262,144 bytes of memory that is I/O mapped. One LS-100 board provides the equvalent storage of an 8 inch single sided single density floppy disk drive.

Four I/O ports are required to control the LS-100 board. These ports are switch selectable to any four consecutive ports of the 256 that are available. There can be up to eight LS-100 boards with the same base I/O port address, providing the user with 2,097,152 bytes of on line storage. If more storage is required, then four more I/O ports will have to be assigned to the next group of eight boards.

Each LS-100 board can address 2,048 128 byte pages or "sectors". In order to address the LS-100 board, the floppy disk track and sector numbers that are provided by CP/M are used by the driver program to generate an address that will support up to eight LS-100 boards. This provides a total of 16,384 128 byte pages or "sectors" of storage.

Data integrity is maintained by a software generated check sum byte that is computed on each 128 byte sector and stored in a reserved area. On each 128 byte sector read, the check sum byte is re-computed and compared with the orginal checksum byte that was generated when the data was stored. If an error condition occurs the user is prompted as to which LS-100 board the error occured on, allowing quick isolation of a fault to the board level.

The LS-100 provides a dramatic speed improvement in disk intensive software by using semiconductor memory for storage instead of magnetic media. Such programs as high level languages like PASCAL, FORTRAN, PL/I-80, etc. will execute from 7 to 10 times faster when compared to a floppy disk drive. Other programs such as editors will also benefit in improved performace when excuted on the LS-100, as these programs frequently use overlays that must be read in from the disk drive. Once you have used the LS-100 you will never want to WAIT on a floppy disk drive again.

* CP/M is a registered trade mark of DIGITAL RESEARCH (California)

TABLE 1-1

1.5 Storage Capacity

The following table provides the storage capacity that can be achived based on the number of LS-100 boards in the system.

Number of Boards	Max. Dir. Entr.	Storage in Kilobytes
1	128 (4k)	254
2	128 (4k)	508
3	256 (8k)	760
4	256 (8k)	1016
5	512 (16k)	1264
6	512 (16k)	1520
7	1024 (32k)	1776
8	1024 (32k)	2032

2.1 GENERAL CONSTRUCTION HINTS

For soldering we recommend a 32 watt soldering pencil. Do not use a soldering gun !!! Use small diameter (such as 22 gauge) rosin core 60/40 alloy solder.

Keep the soldering tip clean with a wet sponge or cloth.

After such components as resistors or capacitors have been soldered, use a small pair of diagonal cutters to remove the excess lead length. CAUTION, WEAR EYE PROTECTION GOGGLES TO PREVENT INJURY TO YOUR EYES.

Observe polarities on all tantalum caps and LEDs.

If you notice any discrepancies between the parts received and those listed, please notify us.

2.3 PARTS LIST

1	40 pin Socket
4	20 pin Sockets
39	16 pin Sockets
7	14 pin Sockets
2	LEDs
3	10 pin SIP resistor packs (3.3k to 4.7k)
1	20 MHZ crystal
4	33 ohm 1/4 watt resistors
2	330 ohm 1/4 watt resistors
1	680 ohm 1/4 watt 5% resistor
1	1k ohm 1/4 watt 5% resistor
2	1N4002 diode
51	.1 mfd Bypass Caps
4	10 mfd. 15 VDC tantalums caps (or larger)
7	6.8 mfd. 10 VDC axial lead caps (or larger)
2	7805 +5 VDC voltage regulaters
2	TO-220 heatsinks with hardware
2	8 position DIP switches
1	4-pin right angle molex connector
2	3 position single row jumper blocks
2	3 position double row jumper blocks
4	shorting plugs
1	printed circuit board
1	74LS00
1	7406 or 7416

PARTS LIST Cont.

1	74S08 (do not substitute)
1	74LS14
1	74LS32
2	74S32 (do not substitute)
1	74LS138
1	74LS139
1	74LS155
2	74LS193
1	74LS244
1	74LS373
2	74LS374
1	74LS367A or 8T97 or DM8097
1	DM8131
1	8203-1
32	MK4564P-20 Mostek 64K Dynamic rams (Orequivalent withanaccess time of 250 ns. or faster.)

(NOTE: C5 and C7 are not supplied with the kit as these caps are only required for fundamental crystals. If a fundamental crystal is used for XY1 then install a 3-10 pf. cap at locations C5 and C7.)

2.3 ASSEMBLY PROCEDURE

[] Give the PC board a good visual inspection for any obvious shorts or opens. There should be none, but a few minutes spent here could save hours later.

[] Using an ohmmeter, insure that there are no shorts between BUS pins 1 and 50.

[] Install and solder 32 16 pin sockets at locations Y1 through Y32. Note that pin #1 is oriented to the top of the PC board.

[] Install and solder 7 16 pin sockets at locations Z3, Z5, Z12, Z13, and Z18-Z20. Note that pin #1 is oriented to the top of the PC board.

[] Install and solder 7 14 pin sockets at locations Z4, Z6, Z9, Z10, and Z15-Z17. Note that pin #1 is oriented to the top of the board.

[] Install and solder 4 20 pin sockets at locations Z11, Z14, Z22, and Z23. Note that pin #1 is oriented to the top of the board.

[] Install and solder the 40 pin socket at location Z7. Note that pin #1 is oriented to the left of the board.

[] Install and solder three 10 pin SIP resistor packs at locations Z8, Z21, and Z24. Pin #1 is up on these parts.

[] Install and solder the four radial lead tantalum caps at locations C1, C2, C3, C4. Please observe the proper polarity when installing these parts.

[] Install and solder the bypass caps in locations C6, and C8-C57.

[] Install and solder seven axial lead caps at locations C58, C59, C60, C61, C62, C63, C64. Please observe the proper polarity when installing these parts.

[] Install and solder the two diodes in locations D1, and D2. Please observe the proper polarity when installing these parts.

[] Install and solder the two LEDs at locations DS1 and DS2. The cathode (denoted by the flat side) goes toward the left side of the board.

ASSEMBLY PROCEDURE Cont.

[] Install and solder the 20 MHZ crystal at location XY1.

[] Install and solder two 330 ohm resistors at locations R5 and R6.

[] Install and solder a 680 ohm resistor at location R8.

[] Install and solder a 1K ohm resistor at location R7.

[] Install and solder four 33 ohm resistors at locations R1, R2, R3, and R4.

[] Install and solder two eight position dip switches at locations S1, and S2. Switch position one is toward the top of the board.

[] Install and solder the four pin molex connector at position B2.

[] Install and solder a single row three position jumper block at locations J1-J2.

[] Install and solder a single row three position jumper block at locations J3-J4.

[] Install and solder a double row three position jumper block at locations J5-J7.

[] Install and solder a double row three position jumper block at locations J8-J10.

[] Using the heatsinks and hardware supplied install and solder the two 7805 voltage regulators at locations Z1 and Z2.

[] Using any of the regulator mounting tabs as ground, measure the output of each 7805 voltage regulator under power in your system. The output is measured on the right pin of the 7805. The measured voltage should be between 4.75 and 5.25 VDC. Any regulator out of spec must be replaced.

[] Install a 74LS00 in socket location Z10. Pin #1 is to the top.

[] Install a 7406 in socket location Z6. Pin #1 is to the top.

[] Install a 74S08 in socket location Z9. Pin #1 is to the top.

ASSEMBLY PROCEDURE Cont.

[ ] Install a 74LS14 in socket location Z16. Pin #1 is to the top.

[ ] Install a 74LS32 in socket location Z17. Pin #1 is to the top.

[ ] Install a 74S32 in sockets locations Z4, and Z15. Pin #1 is to the top.

[ ] Install a 74LS138 in socket location Z3. Pin #1 is to the top.

[ ] Install a 74LS139 in socket location Z5. Pin #1 is to the top.

[ ] Install a 74LS155 in socket location Z18. Pin #1 is to the top.

[ ] Install a 74LS193 in socket locations Z12, and Z13. Pin #1 is to the top.

[ ] Install a 74LS244 in socket location Z22. Pin #1 is to the top.

[ ] Install a 74LS373 in socket location Z23. Pin #1 is to the top.

[ ] Install a 74LS374 in socket locations Z11, and Z14. Pin #1 is to the top.

[ ] Install a 74LS367A in socket location Z19. Pin #1 is to the top.

[ ] Install a DM8131 in socket location Z20. Pin #1 is to the top.

[ ] Install a 8203-1 in socket location Z7. Pin #1 is to the left.

[ ] Install 32 64K Dynamic RAMS in socket locations Y1-Y32. Pin #1 is to the top.

[ ] Install the board in your system and remeasure the voltage regulator outputs to ensure proper operation. (Note: Never install or remove the board when power is applied.)

Board Setup

3.1 I/O BASE PORT ADDRESSING

Dip Switch S-1

A group of four consecutive I/O ports are required to address the LS-100 board. Dip switch S-1 sets the base address of these ports. Switch position 1 corresponds to address bit A7 and switch position 6 corresponds to address bit A2, providing 64 possible base addresses of the 256 that are available. Table 3-1 provides the 64 possible base I/O port addresses. For operation with the supplied software set this switch for base port D0H by setting switches 3,5, and 6 in the on position and switches 1,2, and 4 in the off position. If this conflicts with any other boards in your system then select a new group of I/O ports from Table 3-1, and modify the software accordingly.

3.2 BOARD SELECT

Dip Switch S-2

Dip switch S-2 provides a one of eight board select decode. As more LS-100 boards are installed into the system, each board will have a different board address (i.e. the first board will have switch position 1 closed, the second will have switch position 2 closed etc.) Note that only one switch position on a board should be closed at a time. For board #1, close switch position 1 and open switch positions 2-8.

3.3 JUMPER OPTIONS

3.3.1 Software Power Down Write Protect

J1-J2

If you are going to utilize the stand-by power option to power the LS-100 board when your system is off, then place a jumper at J2. If you chose not to use this option then place a jumper at J1. (Note: When the LS-100 board is power "down write protected" any attempt to read or write to the data transfer port will cause the CPU to lock up until a reset is applied to the CPU.)

JUMPER OPTIONS Cont.

3.3.2 Advanced or Normal Ready

J3-J4

J3

Based on your system requirements, either transfer acknowledge XACK (normal ready) or the system acknowledge SACK (advanced ready) signal can be used to generate the CPU processor ready signal (PRDY). XACK is generally used, however if your system can tolerate an advanced ready, then SACK can be used, but only if the the CPU in your system can tolerate the amount of advanced ready provided by the 8203 controller. If SACK is used no wait states are introduced during data transfers. If XACK is used then two to three wait states are inserted on each data transfer. For normal ready place a jumper at J4. For advanced ready place a jumper at J3. To determine if your system will tolerate an advanced ready, run the diagnostic program. If it will run without any errors then all is probably ok. If you get random errors then you will have to select normal ready. (Note: For more infomation refer to the Memory Components Handbook from Intel on the 8203 Dynamic Ram Controller.)

3.3.3 Refresh Select

J5-J6-J7 J8-J9-J10

J 5 - Internal
J 6 - Refresh
J 7 - Refresh

The 8203 controller has two ways of providing dynamic ram refresh. Internal or External (hidden) refresh. Both types are supported by the LS-100 board. If your processor does not generate a refresh signal such as an 8080 then the internal refresh mode will have to be selected by placing a jumper at J5. However many Z80 processor boards generate a refresh signal. Unfortunately the level and bus pin number used for the refresh signal on older CPU boards is not well defined. The LS-100 board supports both High true and Low true refresh signal levels. If your processor supports Refresh bar (low true) then place a jumper at J7. If your processor supports Refresh (high true) then place a jumper at J6. Bus pins 21, 65, and 66 have been provided for the refresh signal. To use bus pin 21 place a jumper at J10. To use bus pin 65 place a jumper at J9. To use bus pin 66 place a jumper at J8. Note that you not have to use the External refresh mode as the 8203 will provide all refresh cycles as required. However if the External refresh mode is used all data transfers to and from the LS-100 will be at full processor speed. If the Internal refresh mode is used then wait states will be introduced as data transfer cycles and refresh cycles coinside.

Refresh Line
J8 - 66
J9 - 65
J10 - 21

3.4 SETUP CHART FOR 8080 BASED SYSTEMS

I/O PORT BASE ADDRESS D0H

POWER DOWN MODE SELECTED

NORMAL READY SELECTED

INTERNAL REFRESH SELECTED

[ ]	Dip Switch S2	Switch position 1 closed Switch positions 2-8 open	;select board ;#1
[ ]	Dip Switch S1	Switch positions 3,5,6 closed Switch positions 1,2,4 open Switch positions 7,8 not used	;set base ;I/O port ;address to D0H
[ ]	umper at J4		;normal ready
[ ]	Jumper at J2		;select power ;down mode
[ ]	Jumper at J5		;select internal ;refresh mode

3.5 SETUP CHART FOR Z80 BASED SYSTEMS

I/O PORT BASE ADDRESS D0H

POWER DOWN MODE SELECTED

ADVANCED READY SELECTED

EXTERNAL REFRESH ON BUS PIN 66 HIGH TRUE

[ ]	Dip Switch S2	Switch position 1 closed Switch positions 2-8 open	;select board ;# 1
[ ]	Dip Switch S1	Switch positions 3,5,6 closed Switch positions 1,2,4 open Switchpositions 7,8 not used	;set base ;I/O port ;address to D0H
[ ]	Jumper at J3		;Advanced ready
[ ]	Jumper at J2		;Select power ;down mode
[ ]	Jumper at J6		;Refresh ;high true
[ ]	Jumper at J9		;Refresh signal ;on bus pin 66

Table 3-1

3.6 I/O Port Addressing

S-1

Switch Positions (0=closed/1=open)						Base I/O Port Address
1	2	3	4	5	6	
0	0	0	0	0	0	0 0 - 0 3 H
0	0	0	0	0	1	0 4 - 0 7 H
0	0	0	0	1	0	0 8 - 0 B H
0	0	0	0	1	1	0 C - 0 F H
0	0	0	1	0	0	1 0 - 1 3 H
0	0	0	1	0	1	1 4 - 1 7 H
0	0	0	1	1	0	1 8 - 1 B H
0	0	0	1	1	1	1 C - 1 F H
0	0	1	0	0	0	2 0 - 2 3 H
0	0	1	0	0	1	2 4 - 2 7 H
0	0	1	0	1	0	2 8 - 2 B H
0	0	1	0	1	1	2 C - 2 F H
0	0	1	1	0	0	3 0 - 3 3 H
0	0	1	1	0	1	3 4 - 3 7 H
0	0	1	1	1	0	3 8 - 3 B H
0	0	1	1	1	1	3 C - 3 F H
0	1	0	0	0	0	4 0 - 4 3 H
0	1	0	0	0	1	4 4 - 4 7 H
0	1	0	0	1	0	4 8 - 4 B H
0	1	0	0	1	1	4 C - 4 F H
0	1	0	1	0	0	5 0 - 5 3 H
0	1	0	1	0	1	5 4 - 5 7 H
0	1	0	1	1	0	5 8 - 5 B H
0	1	0	1	1	1	5 C - 5 F H
0	1	1	0	0	0	6 0 - 6 3 H
0	1	1	0	0	1	6 4 - 6 7 H
0	1	1	0	1	0	6 8 - 6 B H
0	1	1	0	1	1	6 C - 6 F H
0	1	1	1	0	0	7 0 - 7 3 H
0	1	1	1	0	1	7 4 - 7 7 H
0	1	1	1	1	0	7 8 - 7 B H
0	1	1	1	1	1	7 C - 7 F H

Table 3-1

I/O Port Addressing cont.

S-1 Switch Positions (0=closed/1=open) 1	2	3	4	5	6	Base I/O Port Address
1	0	0	0	0	0	80 - 83 H
1	0	0	0	0	1	84 - 87 H
1	0	0	0	1	0	88 - 8B H
1	0	0	0	1	1	8C - 8F H
1	0	0	1	0	0	90 - 93 H
1	0	0	1	0	1	94 - 97 H
1	0	0	1	1	0	98 - 9B H
1	0	0	1	1	1	9C - 9F H
1	0	1	0	0	0	A0 - A3 H
1	0	1	0	0	1	A4 - A7 H
1	0	1	0	1	0	A8 - AB H
1	0	1	0	1	1	AC - AF H
1	0	1	1	0	0	B0 - B3 H
1	0	1	1	0	1	B4 - B7 H
1	0	1	1	1	0	B8 - BB H
1	0	1	1	1	1	BC - BF H
1	1	0	0	0	0	C0 - C3 H
1	1	0	0	0	1	C4 - C7 H
1	1	0	0	1	0	C8 - CB H
1	1	0	0	1	1	CC - CF H
1	1	0	1	0	0	D0 - D3 H
1	1	0	1	0	1	D4 - D7 H
1	1	0	1	1	0	D8 - DB H
1	1	0	1	1	1	DC - DF H
1	1	1	0	0	0	E0 - E3 H
1	1	1	0	0	1	E4 - E7 H
1	1	1	0	1	0	E8 - EB H
1	1	1	0	1	1	EC - EF H
1	1	1	1	0	0	F0 - F3 H
1	1	1	1	0	1	F4 - F7 H
1	1	1	1	1	0	F8 - FB H
1	1	1	1	1	1	FC - FF H

3.7 BATTERY BACK-UP OPTION

The LS-100 provides a standby power option that can be used to provide power to the LS-100 board when the host computer is turned off. Before the host computer is turned off the Power Down write protect bit should be set to a "1" in the MSB Address Register (Bit 6 of register-1). This will protect the data from being accidentally altered when the host computer is powered up. Note that this bit is set to a "0" when the set sector routine is called in the driver software. An external power source can be connected to the LS-100 board at the 4 pin MOLEX connector B2 located at the top left of the board. Pins 1 and 4 are ground and Pins 2 and 3 are power. A filtered D.C. power source of 8 to 10 volts at 800 MA. per board is required.

3.8 STATUS LED INDICATORS

The LS-100 has two LED status indicators located at the top left center of the board. DSP-1 is the access indicator and is only on during the actual data read and write transfer cycles. DSP-2 is the board select indicator and will stay on as long as the board is selected. These LEDs provide a quick visual check for proper board addressing and operation.

SOFTWARE

4.1 DIAGNOSTIC PROGRAM

The diagnostic program provides a means for verifying that the LS-100 is operational. When excuted the diagnostic program will ask you for the number of the LS-100 board that is to be tested. The memory test will continue to run until interrupted by pressing any key on the console which transfers control to CP/M. A map of the memory array on the LS-100 board will be displayed after each test pass. A "G" indicates a good memory chip and a "B" indicates a failing memory chip. Replace any bad memory chips before continuing.

The diagnostic program provided has a base I/O port address of D0H. If this conflicts with any other boards in your system the diagnostic program will have to be modified. To change the base port address, edit the diagnostic program source file DIAG.ASM and change the PBASE equate statement to the new port address that you have selected.

Assemble the file with ASM or any other compatible assembler and create a COM file. Check all jumper options and dip switch settings, and install the LS-100 board into your system. Be sure all power is off when installing or removing the board. Boot up CP/M and type DIAG$crt, this will load and execute the diagnostic program.

4.1.1 SAMPLE DIAGNOSTIC PROGRAM SESSION

```
AtDIAG
                LS-100  MEMORY  DIAGNOSTIC  PROGRAM

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                          COPYRIGHT 1983
                             VER. 1.0

ENTER NUMBER OF BOARD TO TEST (1-8): 1

PRESS ANY KEY TO EXIT TO CP/M

TEST RESULTS FOR BOARD 1

PASS NUMBER 0001H

        DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
BANK-1   G   G   G   G   G   G   G   G
BANK-2   G   G   G   G   G   G   G   G
BANK-3   G   G   G   G   G   G   G   G
BANK-4   G   G   G   G   G   G   G   G
At
```

SOFTWARE Cont.

4.2 FORMAT PROGRAM

When power is first applied to the LS-100 board the contents of memory will be random data. Before the board can be used it must first be formatted. A format program is supplied with a default base I/O port address of D0H. If this conflicts with any other boards in your system then the format program will have to be modified.

To change the base I/O port address, edit the format source program FMAT.ASM and change the PBASE equate statement to the new port address that you have selected. Assemble the file with ASM or any other compatible assembler and create a FMAT.COM file. Type FMAT$crt to run the format program.

The format program will search for the number of LS-100 boards in your system, automatically format, and then verify the reserved check sum area for an 80H, and the data area for an E5H. This program dynamically formats the LS-100 Boards depending on the number of boards in the system. Therefore as more LS-100 boards are added to the system no further software changes are required.

4.2.1 SAMPLE FORMAT PROGRAM SESSION

```
A>FMAT

                LS-100  AUTO  FORMAT  PROGRAM

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                    ALL RIGHTS RESERVED
                      COPYRIGHT 1983
                        VER. 1.0

FORMATTING 1 LS-100 BOARD(S)
VERIFYING FORMAT
DONE
A>
```

SOFTWARE Cont.

4.3 INSTALL PROGRAM

The Install program is actually two programs combined into one, a relocator program and the driver program. The relocator program is a CP/M com file ORGed at 100H while the driver is ORGed just below the CCP and moved to 1000H (by using DDT). Then the driver and relocator program are saved together as one file with the SAVE command. The actual load address of the driver depends on the CP/M system size (MSIZE) equate, as the install program moves the driver module from 1000H to just below the CCP (CPMB).

After the driver module is in place, the CP/M BIOS jump table is copied to a reserved area within the driver module, and then a modified BIOS jump table with pointers into the driver module is moved to the original BIOS jump table area. This allows the driver module to intercept system calls to the BDOS. The BDOS entry point at memory locations 6 and 7 are then altered to reflect the new TPA size protecting the driver module (hopefuly).

This is how CP/M is tricked into thinking that the LS-100 boards are a disk drive. Before you can run the Install program you will have to edit the Install program and the driver module and set the following EQUATES to match your system. Be sure that both the install program (INSTALL.ASM) and the driver module (DRV1.ASM) have the following identical parameters.

```
PBASE   EQU     (base  I/O port address)

MSIZE   EQU     (size of CP/M in Kilobytes)

DRVID   EQU     (drive #  1-15)
```

After you have assembled the driver and the install program list the the INSTALL.PRN file and obtain the value of DRV1 i.e. for a 60K CP/M SYSTEM DRV1=D000H. Load the install module with DDT as follows. DDT INSTALL.HEX§crt, this will load the Install hex file at 100H. Next using the hex caculator in DDT find the offset of the driver module from 0H. H0,(value for DRV1)§crt. Add 1000 hex to this value and use this offset as follows. IDRV1.HEX§crt R(offset). This will load the driver module at 1000H. Now save the two modules by typing G0 to exit DDT and then type SAVE 17 INSTALL.COM to save the Install program on the logged in drive.

Install program cont.

To execute the install program type INSTALL$crt. The install program will search for the number of LS-100 boards in your system and dynamically install the correct drive parameter block based on the number of boards in the system, automatically increasing the amount of storage provided. (See Table 1-1). Therefore as more boards are added to the system no further software changes are required. The driver module contains a check sum routine which calculates a check byte for each 128 byte page or "sector" that is written to and read from the LS-100 boards. If a check sum error occurs an error message is displayed reporting which board the error occured on. This type of error is most probably caused by a failing memory chip. If this happens it is recommended that the diagnostic program be run on the failing board to locate the memory chip that is having problems.

Customizing the Install program

(This is for a 60K CP/M system)

Edit both DRV1.ASM, and INSTALL.ASM and set MSIZE=60
(Note: the default drive ID is drive E and the default
base I/O port address is D0H)
Assemble DRV1, and INSTALL to obtain a hex file for each
List the ~~DRV1~~ INSTALL.PRN file and obtain the value for DRV1

DRV1 offset value

```
DDT INSTALL.HEX$crt    ;load hex file into memoryat 100H
H0,D000$crt             ;find offset from 0H. (D000H,3000H)
D000,3000              ;add1000Htooffset. (3000H+1000=4000H)
IDRV1.HEX$crt          ;prepare to read in driver module
R4000H$crt             ;read with offset to place at 1000H
G0$crt                 ;exit DDT
SAVE17 INSTALL.COM$crt ;save both install & driver as one file
```

DRV1 →

~~3000~~
~~D200~~
2E00

60K - CA00 - DRV

4.4 INSTALL PROGRAM INCOMPATIBILITIES

The Install program is a fast way to get the LS-100 board up and running, however this method has some inherent problems. As was mentioned above the install program changes the TPA size by reducing the top of memory pointers at locations 6 and 7 which is the BDOS entry point.

Unfortunately some programs may ignore the top of memory pointer and overwrite the driver module. If this happens, a system crash is inevitable. Other problems arise when certain programs do direct disk I/O through the BIOS jump table instead of using the CP/M function calls. Such programs are fast disk copiers.

These types of programs will not function properly as the LS-100 format is different from that of a floppy disk. Use PIP instead to copy files from drive to drive and these problems will be eliminated. Also note that a copy of CP/M does not reside on the reserved tracks as with floppy disk drives. Instead, this area has been reserved for the check sum bytes. To get around the problem of warm booting from the emulated drive, the Driver program modifies the warm boot routine to jump to the CCP which will log in the emulated drive without re-reading in CP/M as the CCP should be protected by the reduced memory pointer at locations 6 and 7. This may cause problems with some BIOS routines that support density changes in the warm boot routine. To eliminate this type of problem we suggest that the LS-100 driver module be integrated into your BIOS.

4.4.1 SAMPLE INSTALL PROGRAM SESSION

```
A>INSTALL

                LS-100  AUTO INSTALL PROGRAM

                DIGITAL RESEARCH COMPUTERS
                   ALL RIGHTS RESERVED
                   COPYRIGHT 1983
                      VER. 1.0

DRIVER INSTALLED FOR 1 LS-100 BOARD(S)

DRIVE E: ACTIVE

A>
```

5.1 HOW TO USE THE LS-100

Every time power is applied to the LS-100 board it must first be formatted before you can use it as a disk drive emulator. To format the LS-100 run the format program FMAT by typing FMAT§crt. Assuming all went well the next step is to install the software driver for the LS-100. To install the driver run the install program by typing INSTALL§crt. The install program as supplied installs the LS-100 board or boards as drive E. Log on to drive E and use the DIR command to look at the directory. There should be no files present. Use PIP to copy a text file to the LS-100 using the verify option. (i.e. PIP E:=A:TEST.TXT[V]) now use the TYPE command to list the text file. Note that not only is the LS-100 faster but it is also silent in operation. Next assemble some programs noting the speed at which they execute. Depending on the number of disk accesses, the execution speed improvement can be from 7 to 10 times faster than that of a floppy disk drive, and typicaly twice as fast as most hard disk drives. The LS-100 provides an economical means of increasing system performance.

6.1 LS-100 I/O PORT REGISTER DESCRIPTION

Control of the LS-100 board is done through four consecutive I/O ports. Their operation is described as follows :

REGISTER-0	DATA TRANSFER PORT	(8 BITS)	READ/WRITE
REGISTER-1	MSB ADDRESS REGISTER	(7 BITS)	WRITE ONLY
REGISTER-2	LSB ADDRESS REGISTER	(8 BITS)	WRITE ONLY
REGISTER-3	BYTE LOCATION REGISTER	(7 BITS)	WRITE ONLY

6.1.1 REGISTER-0 DATA TRANSFER PORT

(BASE ADDRESS+0)

The data port provides the means for transferring data between the host computer and the LS-100 board. Data is transferred by using the processors input and output instructions. Reading or writing to the data port also automatically increments the byte location address register by one, addressing the next byte within the 128 byte page or "sector".

6.1.2 REGISTER-1 MSB ADDRESS REGISTER

(BASE ADDRESS+1)

Register one is a seven bit write only register and provides the most significant address and power down mode selection. Bit 7 of this register is not used and is not connected. Bit 6 when set to a one selects the power down write protect mode. Bits 5 - 3 are address bits A20 - A18 and provide a one of eight board decode. Bits 2 - 1 are address bits A17 - A16 and provides a one of four bank decode. Bit 0 is address bit A15 of the memory array on the LS-100 board. The CPU data bus is not driven when reading from this register.

		A20 - A18			A17-A16	A15
N/C	POWER DOWN WRT PROT	1 of 8 BOARD SELECT			1 of 4 BANK SEL	of MEM ARRAY
7	6	5	4	3	2	1	0

I/O port register description cont.

A15 – REG 1

6.1.3 REGISTER-2 LSB ADDRESS REGISTER

(BASE ADDRESS+2)

A14 – A7 of MEM ARRAY

7	6	5	4	3	2	1	0

Register two is an eight bit write only register. Bits 7 - 0 are memory address bits A14 - A7 to the memory array on the LS-100 board. Writing to this register clears the byte location address counters to zero. The CPU data bus is not driven when reading from this register.

6.1.4 REGISTER-3 BYTE LOCATION ADDRESS REGISTER

(BASE ADDRESS+3)

Register three is an 7 bit write only register which provides the capability to address a byte within a 128 byte page or "sector". Bit 7 of this register is not used and is not connected. Bits 6 - 0 are address bits A6 - A0 to the memory array on the LS-100 board. The CPU data bus is not driven when reading from this register.

A6 – A0 BYTE IN 128 BYTE PAGE OR SECTOR

N/C	6	5	4	3	2	1	0

6.2 BIOS INTEGRATION

An install program has been provided with the LS-100. However it is best to incorporate the LS-100 driver directly into your BIOS. This may or may not be a trival task based on your experience with CP/M and assembly language programming. It is most important that you have a source listing of your BIOS before attempting modification. If you have never modified a BIOS before then obtain a copy of the CP/M alteration guide from DIGITAL RESEARCH. Section 3 of the alteration guide will provide all the nessary information to regenerate your BIOS.

The following examples have been provided to aid the systems programmer to integrate the LS-100 driver module directly into the BIOS.

```
;     DRVID is Equated to the number of the drive that the LS-100
;board will emulate. This should be the next logical drive in
;your system. For a 2 drive system DRVID would be set to 02 for
;drive C.
;
DRVID     EQU       (01-15)          ;DRIVE ID. (B-P)
;
;     The following equates define the LS-100 hardware
;
PBASE     EQU       0D0H             ;DEFAULT BASE PORT ADDRESS
REG0      EQU       PBASE            ;DATA TRANSFER PORT
REG1      EQU       PBASE+1          ;MSB ADDRESS REGISTER
REG2      EQU       PBASE+2          ;LSB ADDRESS REGISTER
REG3      EQU       PBASE+3          ;BYTE LOCATION REGISTER
NBYTES    EQU       128              ;BYTES/TRANSFER (FIXED)
;
;
;
;     This routine checks the active drive byte to see if the BDOS
;is accessing the LS-100 board.
;
CHECK:    LDA       UNIT             ;GET ACTIVE #
          CPI       DRVID            ;CHECK FOR LS-100
          RET
```

```
;
;   The head home routine is modified to check for the LS-100
;board and conditionally skip the floppy disk controller routine.
;The LS-100 board has no head to home however the track byte is
;set to zero.
;
;HEAD HOME ROUTINE
;
HOME:     CALL      CHECK          ;CHECK FOR LS-100
          JZ        HME1           ;JUMP IF LS-100 IS ACTIVE
          .                        ;NORMAL CODE
          .                        ;CONTINUES
          .
HME1:     XRA       A
          STA       TRK            ;SET TRACK TO 0
          RET                      ;NORMAL RETURN

;     The sector translate routine is modified as follows as the
;LS-100 does not require sector translation.
;
;SECTOR TRANSLATE ROUTINE
;
SCTRL:    CALL      CHECK          ;CHECK FOR LS-100
          JZ        SCTRL2         ;JUMP IF SO
          .
          .                        ;NORMAL CODE
          .                        ;CONTINUES
          .
          RET                      ;NORMAL RETURN
;
SCTRL2:   MOV       H,B            ;TRANSLATION
          MOV       L,C            ;NOT REQUIRED
          RET

;
;READ SECTOR ROUTINE
;
READ:     CALL      CHECK          ;CHECK FOR LS-100
          JZ        RD100          ;LS-100 SECTOR READ
          .
          .                        ;NORMAL CODE
          .                        ;CONTINUES
          .
          RET                      ;NORMAL RETURN
```

```
;
;WRITE SECTOR ROUTINE
;
WRITE:    CALL      CHECK          ;CHECK FOR LS-100
          JZ        WR100          ;LS-100 SECTOR WRITE
          .
          .                        ;NORMAL CODE
          .                        ;CONTINUES
          .
          RET                      ;NORMAL RETURN

;    This routine sets up the address registers on the LS-100
;board for a 128 byte page or "sector" data transfer. Also the HL
;register pair is loaded with the DMA address for the transfer.
;Register B is loaded with the number of bytes per page and the
;check sum Register (E) is cleared to zero.
;
;
SETUP:    LDA       TRACK          ;GET CURRENT TRACK #
          OUT       REG2           ;SET LSB ADDRESS REGISTER
          LDA       SECTOR         ;GET CURRENT SECTOR #
          OUT       REG1           ;SET MSB ADDRESS REGISTER
          LHLD      TADDR          ;HL=ADDRESS OF TRANSFER BUFFER
          MVI       B,NBYTES       ;B=BYTES/SECTOR
          MVI       E,0            ;CLEAR CHECK SUM BYTE
          RET
;
;    This routine sets the address registers, and the byte
;location register based on the current track number and sector
;number in preparation to store or retrieve the check sum byte
;that is computed on each 128 byte page or "sector".
;
;
CALC:     LXI       H,TRACK        ;SET HL @ TRACK #
          XRA       A              ;CLEAR A, AND CARRY FLAG
          OUT       REG2           ;SET LSB ADDRESS REGISTER
          MOV       A,M            ;GET CURRENT TRACK #
          RLC                      ;MOD. 128
          JNC       SKP1           ;JUMP IF $128
          MVI       A,1            ;GET RESERVED TRACK #
          OUT       REG2           ;SET LSB ADDRESS REGISTER
SKP1:     MOV       A,M            ;GET CURRENT TRACK #
          OUT       REG3           ;SET BYTE LOCATION REGISTER
          RET
```

```
;
;     This routine reads 128 bytes from the LS-100 board storing
;the data in the memory buffer pointed to by HL  and compares the
;computed check sum byte with the value stored in the reserved
;check sum area on the LS-100 board. The normal CP/M return is
;with the Z flag = 1 and the error return is with the Z flag = 0.
;
;LS-100 SECTOR READ ROUTINE
;
RD100:    CALL     SETUP          ;SETUP REGISTERS FOR TRANSFER
RDLP:     IN       REG0           ;GET DATA FROM LS-100
          MOV      M,A            ;STORE @HL
          ADD      E              ;COMPUTE CHECK SUM
          MOV      E,A            ;ACCUMULATE IN E
          DCR      B              ;DECREMENT BYTE COUNTER
          JNZ      RDLP           ;UNTIL ZERO
          CALL     CALC           ;SETUP ADDRESSOFCHECK SUM BYTE
          IN       REG0           ;GET CHECK SUM BYTE
          SUB      E              ;CHECK FOR ERROR
          RET                     ;SHOULD BE 0

;     This routine writes 128 bytes from the memory buffer
;pointed to by HL to the LS-100 board, computes a check sum byte
;and stores the check sum byte in the reserved check sum area on
;the LS-100 board.
;
;
;LS-100 WRITE SECTOR ROUTINE
;
WR100:    CALL     SETUP          ;SETUP REGISTERS FOR TRANSFER
WRLP:     MOV      A,M            ;GET DATA FROM BUFFER
          OUT      REG0           ;STORE DATA
          ADD      E              ;COMPUTE CHECK SUM
          MOV      E,A            ;ACCUMULATE CHECK SUM IN E
          INX      H              ;INCREMENT POINTER
          DCR      B              ;DECREMENT BYTE COUNTER
          JNZ      WRLP           ;UNTIL ZERO
          CALL     CALC           ;SET UP ADDRESS OF CHECK SUM BYTE
          MOV      A,E            ;GET CHECK SUM BYTE
          OUT      REG0           ;WRITE CHECK SUM BYTE
          XRA      A              ;CLEAR ERROR FLAG
          RET                     ;NORMAL RETURN
```

```
;     The following provides the disk parameter information used
;by the SELDISK routine for 1 LS-100 board. Refer to table 6-1
;for drive parameters for up to 8 LS-100 boards.
;
;(X) IS THE LOGICAL DRIVE NUMBER IE. 1=B/2=C/3=D...ETC.
;
DPE(X):   DW      XLT(X),0000H    ;TRANSLATE TABLE
          DW      0000H,0000H     ;SCRATCH AREA
          DW      DIRBUF,DPB(X)   ;DIR.BUF./PARM. BLOCK
          DW      CSV(X),ALV(X)   ;CHECK ALLOC. VECTORS

DPB(X):   DW        8             ;SECTORS/TRACK
          DB        4             ;BLOCK SHIFT
          DB       15             ;BLOCK MASK
          DB        1             ;EXTNT. MASK
          DW      126             ;DISK SIZE-1
          DW      127             ;MAX. DIRECTORY ENTRIES
          DB      192             ;ALLOC0
          DB        0             ;ALLOC1
          DW        0             ;CHECK SIZE
          DW        2             ;OFFSET


;
;REQUIRED STORAGE MUST BE IN RAM
;
ALV(X):   DS       64             ;ALLOCATION VECTOR FOR 8 BOARDS
CSV(X):   DS        0             ;ZERO CHECKED DIR. ENTRIES
```

6.3 TABLE 6-1 DISK PARAMETER BLOCKS

```
;
;PARAMETERS FOR 1 BOARD
;
DPB(X): DW      8               ;SECTORS/TRACK
        DB      4               ;BLOCK SHIFT
        DB      15              ;BLOCK MASK
        DB      1               ;EXTNT. MASK
        DW      126             ;DISK SIZE-1
        DW      127             ;MAX. DIRECTORY ENTRIES
        DB      192             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET



;
;PARAMETERS FOR 2 BOARDS
;
DPB(X): DW      16              ;SECTORS/TRACK
        DB      4               ;BLOCK SHIFT
        DB      15              ;BLOCK MASK
        DB      1               ;EXTNT. MASK
        DW      253             ;DISK SIZE-1
        DW      127             ;MAX. DIRECTORY ENTRIES
        DB      192             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET
```

TABLE 6-1 Cont.

```
;
;PARAMETERS FOR 3 BOARDS
;
DPB(X): DW      24              ;SECTORS/TRACK
        DB      5               ;BLOCK SHIFT
        DB      31              ;BLOCK MASK
        DB      3               ;EXTNT. MASK
        DW      189             ;DISK SIZE-1
        DW      255             ;MAX. DIRECTORY ENTRIES
        DB      192             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET


;
;PARAMETERS FOR 4 BOARDS
;
DPB(X): DW      32              ;SECTORS/TRACK
        DB      5               ;BLOCK SHIFT
        DB      31              ;BLOCK MASK
        DB      3               ;EXTNT. MASK
        DW      253             ;DISK SIZE-1
        DW      255             ;MAX. DIRECTORY ENTRIES
        DB      192             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET
```

TABLE 6-1 Cont.

```
;
;PARAMETERS FOR 5 BOARDS
;
DPB(X): DW      40              ;SECTORS/TRACK
        DB      6               ;BLOCK SHIFT
        DB      63              ;BLOCK MASK
        DB      7               ;EXTNT. MASK
        DW      157             ;DISK SIZE-1
        DW      511             ;MAX. DIRECTORY ENTRIES
        DB      192             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET



;
;PARAMETERS FOR 6 BOARDS
;
DPB(X): DW      48              ;SECTORS/TRACK
        DB      6               ;BLOCK SHIFT
        DB      63              ;BLOCK MASK
        DB      7               ;EXTNT. MASK
        DW      189             ;DISK SIZE-1
        DW      511             ;MAX. DIRECTORY ENTRIES
        DB      192             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET
```

TABLE 6-1 Cont.

```
;
;PARAMETERS FOR 7 BOARDS
;
DPB(X): DW      56              ;SECTORS/TRACK
        DB      6               ;BLOCK SHIFT
        DB      63              ;BLOCK MASK
        DB      7               ;EXTNT. MASK
        DW      221             ;DISK SIZE-1
        DW      1023            ;MAX. DIRECTORY ENTRIES
        DB      240             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET



;
;DISK PARAMETERS FOR 8 BOARDS
;
DPB(X): DW      64              ;SECTORS/TRACK
        DB      6               ;BLOCK SHIFT
        DB      63              ;BLOCK MASK
        DB      7               ;EXTNT. MASK
        DW      253             ;DISK SIZE-1
        DW      1023            ;MAX. DIRECTORY ENTRIES
        DB      240             ;ALLOC0
        DB      0               ;ALLOC1
        DW      0               ;CHECK SIZE
        DW      2               ;OFFSET
```

7.1 Basic Theory of Circuit Operation

7.1.1 I/O PORT SELECT AND REGISTER DECODE

Z22 buffers data bits D0-D7 from the CPU data bus onto the board. Z20 provides the base port I/O address decode by comparing address bits A2-A7 to the value selected by dip switch S1. When Z20 decodes a valid address, Z20 pin 9 will go low enabling the dual 1 of 4 decoder Z18. Z18,Z15,Z17, and Z10 decode address bits A0, and A1 along with SINP, SOUT, PWR, and PBDIN providing the I/O register read write ports select signals X0-X3.

7.1.2 BYTE LOCATION ADDRESS REGISTER

Z12, and Z13 form a 7 bit loadable counter, that provide address bits AL0-AL6 to Z7. These counters are incremented on each data transfer by the XACK signal from Z7 which is generated by reading or writing to the data transfer port address X0. These counters can also be loaded with a 7 bit value by writing to address X3, or cleared to zero by writing to address X2.

7.1.3 MSB, LSB ADDRESS REGISTER AND BOARD SELECTION

When the CPU writes to address X2, Z11 will latch D0-D7 providing address bits AL7, and AH0-AH6 to Z7. When the CPU writes to base address X1, Z14 will latch data bits D0-D7, providing AH7, and B0 to Z7. Z14 also provides a 3 bit address to Z3. Z3 along with dip switch S2 provide a 1 of 8 board selection. When Z16 pin 9 is low status LED DS2 will be on indicating that the board is selected, and also enabling the read and write request signals to Z7.

7.1.4 RAS SIGNAL DECODE AND WAIT STATE GENERATION

Z5, Z4, and Z9 provides the 1 of 4 RAS bank decode signals RAS0-RAS3 to the memory array. Z7, and Z6 introduce the necessary wait states by holding the PRDY signal low until valid data is read out of the memory by Z7. DS1 provides an access indicator by monitoring the state of the on board ready signal. Z23 latches the data that is read out of the memory array and drives the DATA IN bus (DI0-DI7) to the CPU.

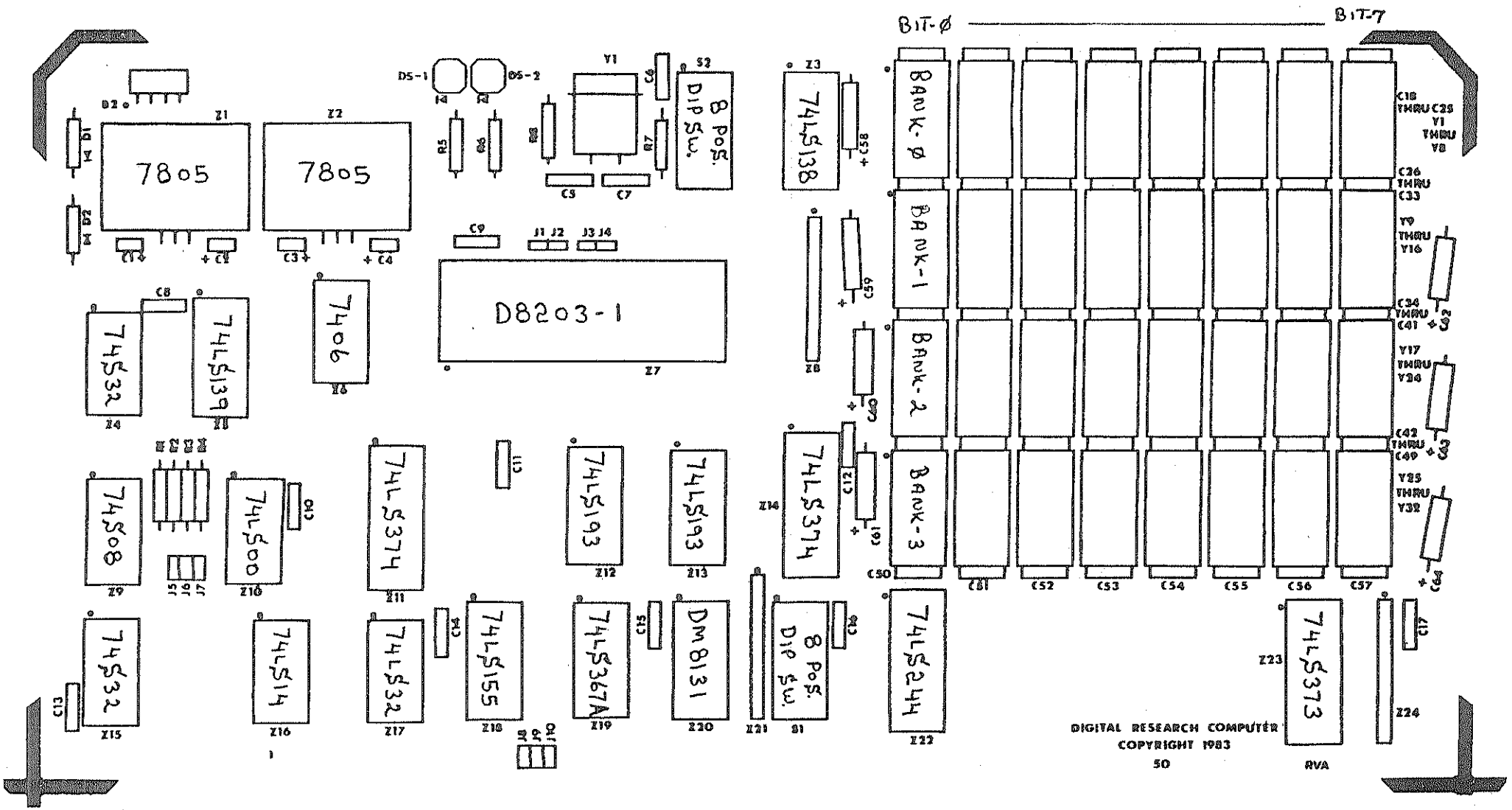
7.1.5 DYNAMIC RAM MEMORY CONTROL

The 8203 controller (Z7) provides all timing and addresses to the 64K dynamic rams, for more information on the operation of the 8203 Dynamic ram controller refer to the Intel Memory Components Handbook.

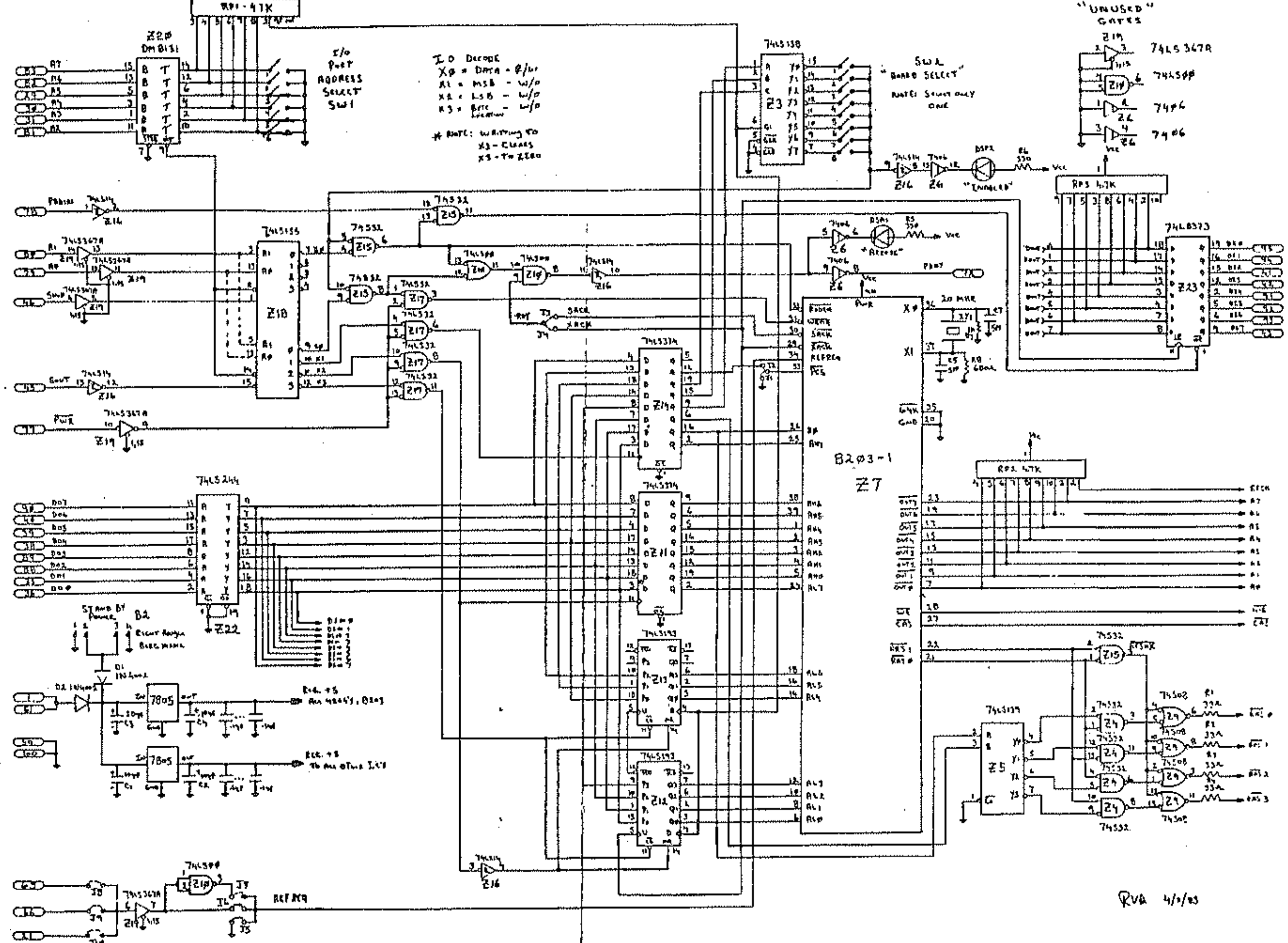
ERROR MESSAGES

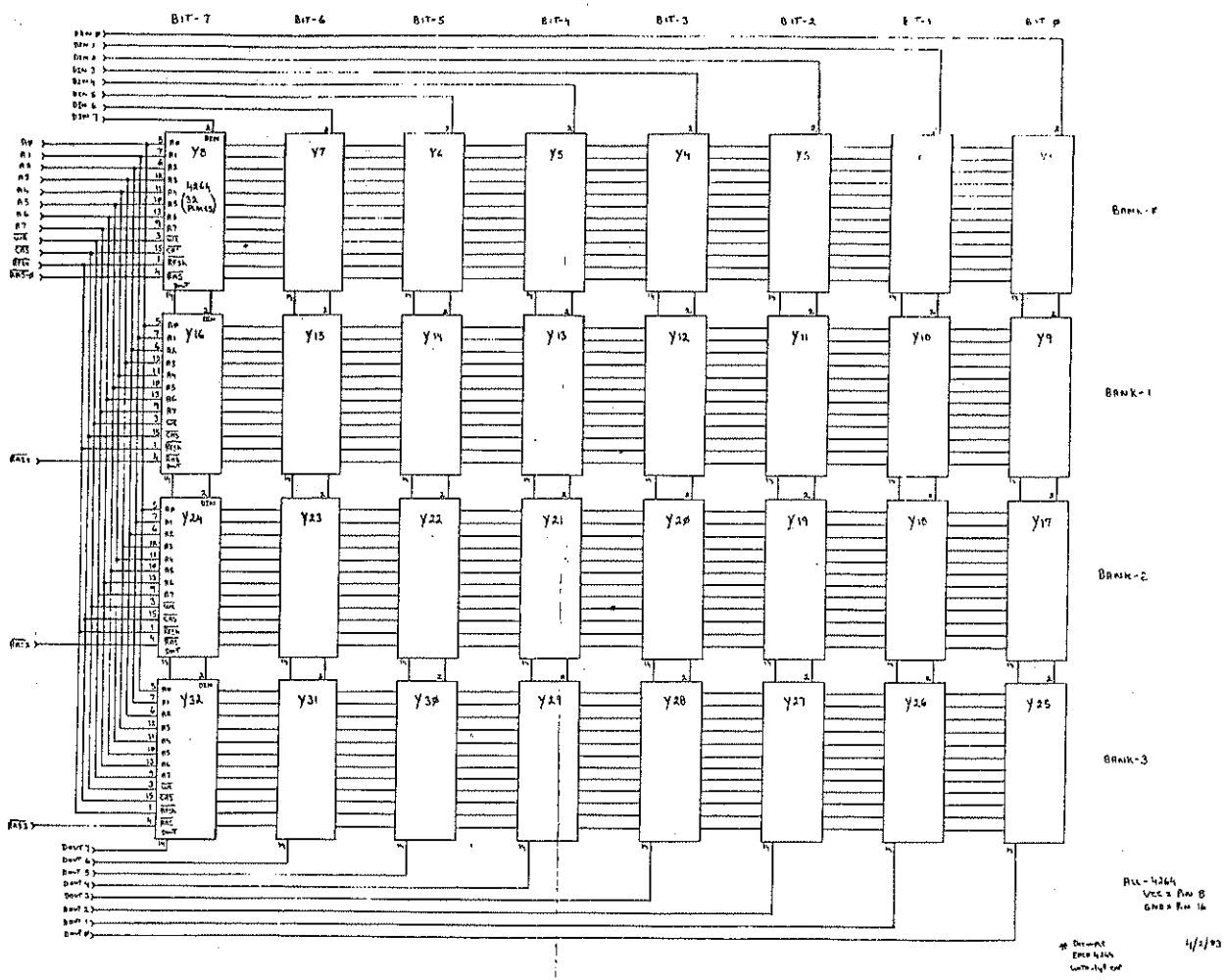
Error Message	Meaning
NO BOARDS FOUND	No LS-100 boards could be located in the system. Check dip switchs S-1 and S-2 to be sure that they are set to the values as equated in the driver and install programs.
NUMBER OF BOARDS FOUND EXCEED LIMIT	The maximun number of LS-100 boards allowed to a group of I/O ports is 8. Check to be sure that no other boards in thesystemare using any of the I/O ports that you have selected for the LS-100 boards.
RELOCATION ERROR CAN°T LOAD DRIVER	The install program checks memory locations 6 and 7 for the BDOS value as equated in the software. Either the CP/M size is equated wrong or another overlay program has changed the top of memory pointer at locations 6and 7.
CP/M 2.0 OR BETTER REQUIRED	CP/M Ver. 2.0 - 2.2 is required in order to use the install program and driver overlay.

MK4564P-20


BIT-Ø
BIT-7
BANK-Ø
BANK-1
BANK-2
BANK-3
7805
7805
8 Pos. DIP SW.
8 Pos. DIP SW.
D8203-1
74LS138
74LS32
74LS139
7406
74LS08
74LS00
74LS374
74LS193
74LS193
74LS374
74LS32
74LS14
74LS32
74LS155
74LS367A
DM8131
74LS244
74LS373
DIGITAL RESEARCH COMPUTER
COPYRIGHT 1983
50
RVA

"256K LS-100"


I/O Port Address Select SW1
I O Decode
X0 = Data - R/W
X1 = MSB - W/O
X2 = LSB - W/O
X3 = Bit Location - W/O
* Note: Writing to X3 - Clears X3 - to Z280
SW2 "Board Select"
Note: Select only one
"Unused" Gates
74LS367A
74LS00
7406
B203-1
Z7
74LS244
74LS155
74LS138
74LS374
74LS373
74LS139
7805
RP1 4.7K
RP2 4.7K
RP3 4.7K
20 MHz
Refresh
RVA 4/?/83


BIT-7
BIT-6
BIT-5
BIT-4
BIT-3
BIT-2
BIT-1
BIT-0
BANK-0
BANK-1
BANK-2
BANK-3
RAS0
RAS1
RAS2
RAS3
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
Y12
Y13
Y14
Y15
Y16
Y17
Y18
Y19
Y20
Y21
Y22
Y23
Y24
Y25
Y26
Y27
Y28
Y29
Y30
Y31
Y32
ALL - 4264
Vcc = Pin 8
GND = Pin 16
4/2/93